Amendments to the Drawings:

The attached replacement sheets of drawings includes changes to Figures 1 and 2 and replaces the original sheet including Figures 1 to 4.

In each of Figures 1 and 2, the legend "(PRIOR ART)" has been added, as suggested by the Examiner.

Attachments following last page of this Amendment:

Replacement Sheet (2 pages)

REMARKS

Applicant thanks the Examiner for the telephone interview dated July 17, 2009, in which amended claims 1 and 30, and the Edwards reference were discussed.

The comments of the Applicant below are each preceded by related comments of the Examiner in the Office Action dated April 21, 2009 (in small, bold type).

Regarding claim 1, Edwards discloses a digital to analogue converter (8-bit DAC 10 of Fig. 1 - see, title, abstract, and col. 3, lines 7-9) comprising:

a plurality of digital inputs (DO-D5 = 6-LSB bits of the 8-bit DAC 10 3 col. 3, lines 7-9) corresponding in number to the number of bits of a digital input word (serial data at terminal 16 of Fig. I), the inputs (6-LSB bits) being used to select one of first and second binary voltage levels (VI and Vh provided by 34 of Fig. 1 3 col. 3, lines 22-25) (VH,VL) as binary inputs to the converter;

a respective capacitor circuit (C, 2C, ..., 32C of weighted capacitor bank or network 20 of Fig. 1) associated with each input (col. 3, lines 23-41);

first and second clock inputs (CKI, CK2 - control line 44 of Fig. 1 3 col. 3, lines 42-48, and col. 4, lines 10-13);

an output load (Cc of Fig. 1 - col. 3, lines 38-41); and

a plurality of switches (charging switches 36 and output switches 42 of Fig. 1) controlled by the clock inputs (on the control line 44) for controlling the coupling of the capacitor circuits either to one of the binary inputs or to the output load (col. 3, lines 42- 48, and col. 4, lines 10-13),

wherein a plurality of the capacitor circuits (including the weighted capacitor network 20 and switches 32, 36, and 42 of Fig. I) are controllable to output an effective voltage to the load comprising the first binary voltage level, the second binary voltage level or an average of the first and second binary voltage levels in dependence on the bits of the digital input word (col. 3, lines 14-67; col. 1, lines 4-18).

Edwards does not describe and would not have made obvious "wherein each of the capacitor circuits is controllable to output an effective voltage to the load, the effective voltage being selectable from at least three voltage levels comprising the first binary voltage level, the second binary voltage level or an average of the first and second binary voltage levels in dependence on the bits of the digital input word," as recited in amended claim 1.

Edwards discloses a digital to analog converter 10 in which a pair of voltage levels Vh, Vl is supplied to a switching network 30 depending on the digital levels of the two most significant bits 12a, 12b of a digital input signal, and each switching device 32 couples a respective output of the switching network 30 to one or other of the voltage lines Vh, Vl. The outputs of the switching network 30 are coupled to a capacitor network 20 having a weighted capacitor bank.

In Edwards, each switching device 32 can be controlled to output a voltage selectable from two voltage levels: Vh and Vl. Edwards does not disclose or suggest that each capacitor circuit is controllable to output an effective voltage to the load, the effective voltage being selectable from at least three voltage levels comprising the first binary voltage level, the second binary voltage level or an average of the first and second binary voltage levels, as recited in claim 1.

> **Regarding claim 30, Edwards discloses a method of performing digital to analogue conversion (see, DAC of Fig. I), comprising:**
>
> **using the bits of a digital input word (8-bit input - col. 3, lines 5-1 0) to generate a plurality of control voltages (col. 3, lines 14-22) corresponding in number to the number of bits (two MSB bits), one control voltage comprising a first binary voltage level or a second binary voltage level, and each other control voltage comprising a first binary voltage level, a second binary voltage level or an average of the first and second binary voltage levels (col. 3, lines 5-22); and**
>
> **using the plurality of control voltages (V1 . ..V5) to drive an output load (load that is connected to node 50 of Fig. 1 - col. 3, lines 35-48).**

Edwards does not describe and would not have made obvious "each other control voltage being selectable from at least three voltage levels comprising a first binary voltage level, a second binary voltage level or an average of the first and second binary voltage levels," as recited in amended claim 30.

Edwards discloses a digital to analog converter 10 in which each of a plurality of switching device 32 couples a respective output of a switching network 30 to one or other of two voltage lines Vh, Vl. Edwards does not disclose or suggest "each other control voltage being selectable from at least three voltage levels comprising a first binary voltage level, a second binary voltage level or an average of the first and second binary voltage levels," as recited in claim 30.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in

which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

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Respectfully submitted,

Date: July 20, 2009

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